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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,802	12/22/2000	Michihide Kimura	1448.1007	9060

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,802	KIMURA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,13-18,20-22 and 24-28* is/are pending in the application.

4a) Of the above claim(s) *12,19,23 and 29-31* is/are withdrawn from consideration.

5)☒ Claim(s) *see parageaph 5* is/are allowed.

6)☒ Claim(s) *see paragraph 9-20* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Clams 1-6,13-18,20-22,24-28 are presented for examination. Claims 1,7-12,19,23,29-31 have been canceled. Claims 13-18, 20-22, 24-28 were previously indicated allowable over the art of record. However, upon further review claims 17 and dependent claims 13,14 are found unpatentable over Hartnett (6, 167, 479) , and unpatentable over Hartnett (6,167,479) in view of Heisch (5,774,724) .

2. The indicated allowability of claim 17 is withdrawn in view of the newly discovered reference(s) to see references above. Rejections based on the newly cited reference(s) follow.

3. This is a non-final action in order to allow applicant a chance to respond. Claim 32 is newly added , and is also rejected over newly found art Hartnett (6,167,479) in view of Takano et al. (5,070,473) .

4. The response and argument filed on 11/14/05 by applicant has been fully considered but is moot in view of newly found art (see Hartnett (6,167,479) in view of Takano et al. (5,070,473)) as to claim 32, and with following effects :

5. Clams 2-6, 20-22, 24-28 are allowable over the art of record as indicated below.

6. Claims 2-6 are allowable as indicated in the previous action.

7. Claims 20-22 are allowable over the art of record . None of the prior art or record teaches combined features of :

a) the exception detection flags, the specific application purpose instruction execution setting the valid sate , notification of the interrupt control due to the operation exception of instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag invalidating instruction and invalidation the exception detection flag (claim 20),

b) the exception detection flags, the specific application purpose instruction execution setting the valid sate , notification of the interrupt control due to the operation exception of the instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag read instruction (claim 21) ;

c) the exception detection flags, the specific application purpose instruction execution setting the valid sate , notification of the interrupt control due to the operation exception of the instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag write instruction (claim22) .

8. Claims 24-28 are allowable over the art of record for reciting the combined features of the condition code register and the branch/interrupt return instruction control unit for determining the interrupt generation based on the value held in the condition code register and the value in the instruction field during the execution of the trap instruction, and the notification that the interrupt is to be generated.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 13,14, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Hartnett (6,167,479).

10. As to claim 17, Hartnett taught at least :

a) a saving of the context after the execution of a program interrupted (e.g. see col.11, lines 5- 37);

b) confirmation unit to confirm whether or not the operation exception had detected during the specific application purpose operation instruction (e.g. see the interrupt type in col.10, lines 51-53, see also the state reflecting the fault and non-fault type interrupt in col.11, lines 5-37, see also determination of what caused the interrupt in col.12, lines 5-8, the specific application - purpose instruction was already taught in 7, lines 41-65).,

c) exception processing unit which carried out exception processing when the exception was detected (e.g. see the interrupt handler in col.12, lines 5-51);

d) return unit returning from interrupt (e.g. see col.12, lines 10-51, see 17, lines 27-40, see also the return instruction in 01.15, lines 44-56, col.17, lines 1-40).

11. Harnett did not explicitly show the storage of the instruction address which interrupted the execution to detect the exception as claimed. Hartnett only disclosed the saving of the context after the execution of a program interrupted (e.g. see col.11, lines 5- 37). However, the examiner holds that the context saved in Hartnett should be applicable generally to any information used in the system, such as the value or a flag used for indicating the instruction address which interrupted the execution. Since no specific type of instruction address has been defined in the specification , nor recited in the claim, the instruction address is read as a context information in general. Applicant is welcome to provide feedback.

12. As to claim 13, Hartnett also included confirmed instruction for breaking (see the interrupt type in col.10, lines 51-53, see also the state reflecting the fault and non-fault type interrupt in col.11, lines 5-37)

13. As to claim 14, , Hartnett also included a memory for storing the exception (see the interrupt state 252 in fig.7).

14. Claim 17 is also rejected under Hartnett (6,167,479) in view of Heisch (5,774,724) to address the storage of the value or a flag for indicating the instruction address interrupted.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 13,14, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett (6,167,479) in view of Heisch (5,774,724) .

16. As to claim 17, Hartnett taught at least :

a) a saving of the context after the execution of a program interrupted (e.g. see col.11, lines 5- 37);

b) confirmation unit to confirm whether or not the operation exception had detected during the specific application purpose operation instruction (e.g. see the interrupt type in col.10! lines 51-53, see also the state reflecting the fault and non-fault type interrupt in col.11, lines 5-37, see also determination of what caused the interrupt in col.12, lines 5-8, the specific application - purpose instruction was already taught in 7, lines 41-65).,

c) exception n processing unit which carried out exception processing when the exception was detected (e.g. see the interrupt handler in col.12, lines 5-51);

d) return unit returning from interrupt (e.g. see col.12, lines 10-51, see 17, lines 27-40, see also the return instruction in 01.15, lines 44-56, col.17, lines 1-40).

Hartnett did not specifically show the storage of the value or the flag indicating the instruction address which was interrupted the execution of the program which was to detect the exception as claimed. However, Heisch disclosed a system for saving instruction address from where the interrupt occurred for exception detection (see col.9, lines 8-15). It would have been obvious to one of ordinary skill in the art to use Heisch in Hartnett for including the storage of the value or the flag indicating the instruction address which was interrupted as claimed because the use of Heisch could provide Hartnett the ability to recover the execution path form where the interrupt occurred, and it could be done by predefining the instruction address with modified control fields , such as the length of the instruction address, in the configuration file of Harnett so that the specific instruction address of Heisch could be recognized by Hartnett for recovering purpose at the interrupt detection, and because Hartnett did disclosed a confirmation of an exception (see the interrupt type in col.10! lines 51-53, see also the state reflecting the fault and non-fault type interrupt in col.11 , lines 5-37, see also determination of what caused the interrupt in col.12, lines 5-8, the specific application - purpose instruction was already taught in 7, lines 41-65), which was a suggestion of the need for storing the interrupted instruction address in order to resume the execution path , and for doing so, provided a motivation.

17. As to claim 13, Hartnett also included confirmed instruction for breaking (see the interrupt type in col.10, lines 51-53, see also the state reflecting the fault and non-fault type interrupt in col.11 , lines 5-37)

18. As to claim 14, , Hartnett also included a memory for storing the exception (see the interrupt state 252 in fig.7).

19. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett (6,167,479) in view of Takano et al. (5,070,473) .

20. As to claim 32, Hartnett taught at least :

a) a control unit (microcontroller 178) for processing an operation instruction (see e.g. the expanded-cycle instruction) as a specific application-purpose operation (e.g. see the microcode controller controlling the instruction execution in col.9, lines 1-23, see also col.7, lines 39-55, col.d, lines 1-13 for the microcode controller during the extended cycles);

b) a specific application-purpose instruction operating unit (e.g. fig.6 (12) IP) for supporting a flexible pipeline structure (see the pipeline processing in col.8, lines 27-43) and capable of being designed to carry out an operation (e.g. address generation) of the specific application-purpose instruction for each application field.

Hartnet did not specifically show the rewritable register for prescribing the instruction latency parameter as claimed. However, Takano disclosed a system including a writable register for prescribing instruction latency parameter (see the number of wait cycles as the parameters in col.5, lines 5-15). It would have been obvious to one of

ordinary skill in the art to use Takano in Hartnett for including rewritable register for prescribing instruction latency parameter as claimed because the use of Takano could provide Hartnett the control capability of Hartnett to halt the instruction processing as long as the number of wait cycle specified by Takano's register, and therefore , providing flexibility of the instruction execution under system abnormal conditions (e.g. the exceptions, faults etc.), and Hartnett did disclose abnormal system condition (see exception), and in doing so , provided a suggestion.

21. Claims 15,16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the detailed functions of the storage and conformation of the operation state in claim 15, and the generation and the confirmation operation state in claim 16.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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